DETAILED ACTION

Specification

A substitute specification filed 9/27/2005 to include priority claim from the provisional application No. 60/245.942 is acknowledged.

Drawings

A replacement sheet of drawings was received on 9/27/2005. The drawings are Fig. 2.

Response to Arguments

Applicant's arguments filed 9/27/2005 with respect to claims 7-10 & 13-16 have been considered but are moot in view of the new ground of rejection.

Applicant's arguments filed 9/27/2005 with respect to claims 1 & 2 have been considered but are not persuasive.

Regarding claim 1, the Applicant asserts, "drawing 400 of the Patent '106 clearly indicates that no MOS gate is present in the region 320 over the punch through transistor region." (remarks, page 8). However, the currently amended claim I does not require any MOS gate. Juiporlan/ly, claim I recites the gate' and '-the source" which lead to a broad interpretifrion of any gate and source region of a vertical punch through transistor (VPT) since the claim clues not specifically exclude any junction gate region that is connected to the source. From this view, the claimed "the gate" is considered as any gale including a junction gate portion of the vertical punch-through transistor as claimed in claim 3 of the Patent '106. For illustration, the Patent '106 clearly supports the claimed feature in claim 3 in col. 4, lines 42-45 that the photo-charge seusing VPT transistor 203 (Fig. 2) is formed in the opening 320 (Fig. 4), and the transistor consists of p+ t~pC (loped source region 405 that is surrounded and connected to the p+ type doped first junction gate region 404. It is also seen that the gate (404) being conductively connected to the source (405) since both the gate and source are doped by the same impurity type (p+) as claimed in claim 3 of the Patent ~l06. Thus, the limitation "a vertical punch-through transistor having the gate surrounding the source and being connected to the source." recited in claim 1 is met by claims & 3 of the Patent ~l06 In addition, claim 7 (a new ground of rejection) is also met by claims 1 & 3 of the Patent '106 for the same reason provided above.

Regarding claim 2, the Applicant states that Kubo Kazuya does not show a vertical punch-through transistor with a gate surrounding its source and being connected to it (remarks, page 9). In response, the Examiner respectfully submits that such feature of the vertical punch- through transistor is taught in the primary reference to the Patent '106. Kubo Kazuya is relied upon for a teaching of a chare present under the gate to modulate the punch through potential barrier of the vertical punch-through transistor (see previous Office Action, pages 6 & 7).

Additionally, the Applicant frirther states, for claim 10, that Lee does not show any structure similar to present invention of a MOS gate surrounding the source and being connected to it (remarks. page 10). In response, the Examiner respectftilly submits the same analysis as in claim 2. Furthermore, claim 10 requires another gate (MOS reset gate) coupled to the vertical punch-through transistor to remove charge therefrom, Lee is relied upon for specific teaching of a MOS reset gate coupled to a transistor to remove charge therefrom in an image sensor (see previous Office Action, pages 8 & 9).

Claim Objections

Comments of the Examiner

Claims 1,7 & 10 are objected to because of the recitation of'..having the gate surrounding the source and being conductively connected to the source." This limitation should be changed to -- having a gate surrounding a source and being conductively connected to the source.

Appropriate correction is required.

Reply to the Examiner's Comments

Claims 1, 7 and 10 have been amended as suggested by the Examiner.

Double Patenting

Comments of the Examiner

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See lure Goodman, II F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, hire Thoringion. 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Claims I & 7 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 3 of U, S. Patent No. 6,580,106 82 (hereafter, referred as Patent '106). Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 1 & 7 of the instant application are encompassed by claims I & 3 of the Patent '106. It should be noted that limitation "the gate surrounding the source and being conductively connected to the source" recited in each of claims 1 & 7 of the instant application is met by "the source of the vertical punch-through transistor... is connected to a first junction gate region surrounding the source and doped by the same impurity type as the source and as the substrate." Also, see the Examiner's response to arguments above.

Claims 2 & 8 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims I and 3 of the Patent '106 in view of Kubo Kazuya (JP 61-188965).

Regarding claims 2 & 8, the claimed invention of Patent '106 does not c/early disclose a charge present under the gate modulates the punch through potential barrier of the vertical punch-through transistor. It is taught by Kubo that a barrier height of a vertical punch through transistor (Fig. I) is modulated by the charges present under the gate (4, 7) to implant excess charge into substrate I for suppressing a blooming, expanding a dynamic range and improving the S/N ratio. See Abstract and Fig. 1.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the feature of modulating the punch through potential barrier of the vertical punch-through transistor by a charge present under the gate for suppressing ablooming, expanding a dynamic range and improving the S/N ratio.

Claims 3. 9, 10 & 13-16 are rejected under thejudicially created doctrine of obviousness- type double patenting as being unpatentable over claims I and 3 of the Patent 106 and Kubo Kazuya (JP 61-188965) and in further view of Lee et al (US 5,904,493).

Regarding claims 3 & 9, the claimed invention of the Patent '106 and Kubo do not clearly teach a charge reset means adjacent to and coupled to the vertical punch-through transistor to remove charge therefrom. However, as taught by Lee, an image sensor having a charge-sensing transistor (at gate Tx) and a charge reset means (reset gate 24: Fig. 4) adjacent to and coupled to the charge-sensing transistor to remove charge therefrom to avoid anti-blooming (see Lee, col. 3, line 65 — col. 4, line 9).

Therefore, it would have been obvious to one of ordinary skill in the an to provide a charge reset means adjacent to and coupled to the vertical punch—through transistor in the claimed invention of the Patent '106 and Kubo to remove charge therefrom to further improve anti-blooming of charge as taught by Lee.

Regarding claim 10, it is clear that the charge reset means is an MOS reset gate (see Lee, col. 3, line 65 — col. 4. line 9).

Regarding claim 13, see the analyses of claims I and 7 for all limitations of claim 13 except for a CCD device. Lee teaches an optimized image sensor that is implemented with best features from both CMOS and CCD technologies. The image sensor improves the blue response and dark current limitations. The image sensor can be called either as CMOS or CCD device. See Lee, col. 1. lines 45-59.

Therefore, it would have been obvious to one of ordinary skill in the art to construct the image sensor having best features from both CMOS and CCD technologies to improve the blue response and dark current limitations of the image sensor which would be either called as a CMOS or a CCD device.

Regarding claims 14-16, see the analyses of claims 8-10, respectively.

Conclusion
Comments of the Examiner

Since all currently pending claims 1-3, 7-10 & 13-16 are rejected under obviousness- type double patenting without a separate art rejeciioii under 35 USC 102 or 103. claims 1, 3, 7-10 & 13-16 will be allowed if a proper terminal disclaimer is filed.

Reply to the Examiner

A terminal disclaimer is enclosed. In view of this, the claims should be allowed, and the application passed to issue.

Respectfully submitted,

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